

What is claimed is:

1 1. A method for testing signals of integrated circuits
2 (ICs), comprising the steps of:

3 successively driving, by a first IC chip, a plurality
4 of test patterns one at a time;

5 receiving, at a second IC chip, and latching in the
6 test patterns one by one;

7 determining, by the second IC chip, whether a currently
8 latched test pattern is correct;

9 if at least an error bit occurs in the currently
10 latched test pattern, the second IC chip
11 indicating that there exists noise interference
12 in a signal trace corresponding to the error bit;
13 and

14 repeating the above steps until the first IC chip
15 finishes driving the test patterns.

1 2. The method of claim 1 wherein the test patterns are
2 at least divided into three types including a ground bounce
3 type, a power bounce type and a heavy load type.

1 3. The method of claim 2 further comprising the step
2 of:

3 if the currently latched test pattern is incorrect, the
4 second IC chip adjusting a reference voltage
5 level in accordance with the type of the
6 corresponding test pattern to change an input
7 threshold of the second IC chip.

1 4. The method of claim 3 wherein the reference voltage
2 level is decreased to lower the input threshold of the
3 second IC chip if the corresponding test pattern belongs to
4 the power bounce type.

1 5. The method of claim 3 wherein the reference voltage
2 level is increased to raise the input threshold of the
3 second IC chip if the corresponding test pattern belongs to
4 the ground bounce type.

1 6. The method of claim 3 wherein the reference voltage
2 level is adjusted in a unit of 0.01 volts at a time.

1 7. The method of claim 3 wherein the reference voltage
2 level is adjusted by changing an internal register setting
3 of the second IC chip.

1 8. The method of claim 1 further comprising the step
2 of:

3 adjusting a driving capability of a pin relative to the
4 error bit for the first IC chip to change the
5 pin's output timing.

1 9. The method of claim 8 wherein the driving
2 capability of the pin relative to the error bit is increased
3 to advance the pin's output timing for the first IC chip.

1 10. The method of claim 8 wherein the driving
2 capability of the pin relative to the error bit is decreased
3 to delay the pin's output timing for the first IC chip.

1 11. The method of claim 8 wherein the output timing is
2 changed in a unit of 150 ps at a time when adjusting the
3 pin's driving capability for the first IC chip.

1 12. The method of claim 8 wherein the output timing is
2 adjusted by changing an internal register setting of the
3 first IC chip.

1 13. A method for testing signals of integrated circuits
2 (ICs), comprising the steps of:

3 receiving a plurality of test patterns and latching in
4 the test patterns on by one through an agent in
5 the integrated circuits;

6 determining, by the agent, whether a currently latched
7 test pattern is correct; and

8 if at least an error bit occurs in the currently
9 latched test pattern, the agent indicating that
10 there exists noise interference in a signal trace
11 corresponding to the error bit.

1 14. The method of claim 13 wherein the test patterns
2 are at least divided into three types including a ground
3 bounce type, a power bounce type and a heavy load type.

1 15. The method of claim 14 further comprising the step
2 of:

3 if the currently latched test pattern is incorrect, the
4 agent in the integrated circuits adjusting a
5 reference voltage level in accordance with the
6 type of the corresponding test pattern to change
7 an input threshold of the agent.

1 16. The method of claim 15 wherein the reference
2 voltage level is decreased to lower the input threshold of
3 the agent if the corresponding test pattern belongs to the
4 power bounce type.

1 17. The method of claim 15 wherein the reference
2 voltage level is increased to raise the input threshold of
3 the agent if the corresponding test pattern belongs to the
4 ground bounce type.

1 18. The method of claim 15 wherein the reference
2 voltage level is adjusted in a unit of 0.01 volts at a time.

1 19. The method of claim 15 wherein the reference
2 voltage level is adjusted by changing an internal register
3 setting of the agent.

1 20. The method of claim 15 further comprising the step
2 of:

3 adjusting a driving capability of a pin relative to the
4 error bit for the agent to change the pin's
5 output timing.

1 21. The method of claim 20 wherein the driving
2 capability of the pin relative to the error bit is increased
3 to advance the pin's output timing for the agent.

1 22. The method of claim 20 wherein the driving
2 capability of the pin relative to the error bit is decreased
3 to delay the pin's output timing for the agent.

1 23. The method of claim 20 wherein the output timing is
2 changed in a unit of 150 ps at a time when adjusting the
3 pin's driving capability for the agent.

1 24. The method of claim 20 wherein the output timing is
2 adjusted by changing an internal register setting of the
3 agent.